Impulse Radio UWB System Architecture for Smart Wireless Sensor Networks

Second International Workshop Networking with UWB
Workshop on Ultra Wide Band for Sensor Networks

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OUTLINE

- Applications
- Requirements
- Sensor Node System Design
- Sensor Heads
- Transmitter architecture
- Receiver architecture
- Positioning

Wireless Sensor Network Applications

- Intelligent Wireless Sensor Networks
  - Threat detection
  - Environmental monitory
  - Civil structures monitory
  - Industrial risks detection
  - ….

Wireless Sensor Network Requirements

- Intelligent Wireless Sensor Networks
  - Ad-hoc networks
  - Multi-hop
  - Reduced size
  - Low power consumption
  - Self configurable routing
  - Able to handle location information
  - Scalable
  - Interference and jamming robust
  - Economically feasible…

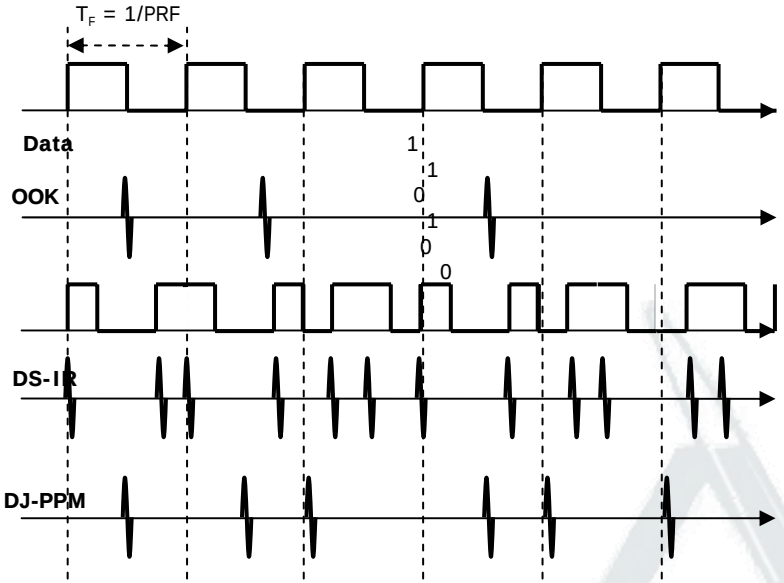
Sensor Node System Design

- Nodes characteristics
  - Communication flow
    - Multihop scheme
      - Power saving
      - Distributed computing requirements
  - Estimate relative position
    - No GPS or Galileo positioning in nodes
  - Security applications:
    - UWB difficult to intercept → Noise like characteristics
    - Robust in hostile electromagnetic environment

Operational mode & Modulation

- Simple design & low cost
  - Fast half-full duplex mode
  - Node hierarchy (reduce power consumption & cost)
    - Share radio module & sensor head
    - Vary procesor core
- Modulation

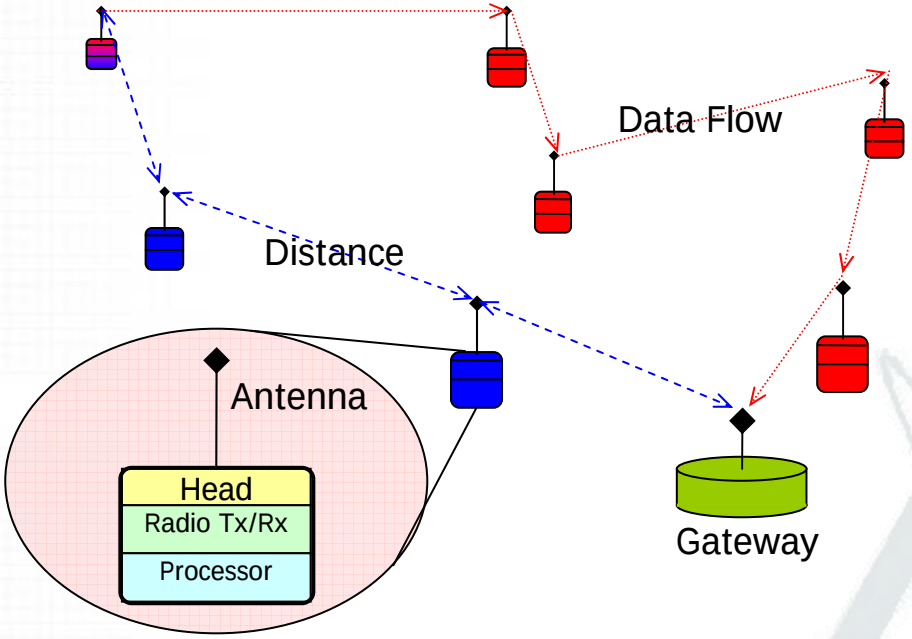
  OOK



Sensor Node System Design

- Location & positioning
- Communication capabilities
- Low cost / low power …

IR-UWB Tecnology

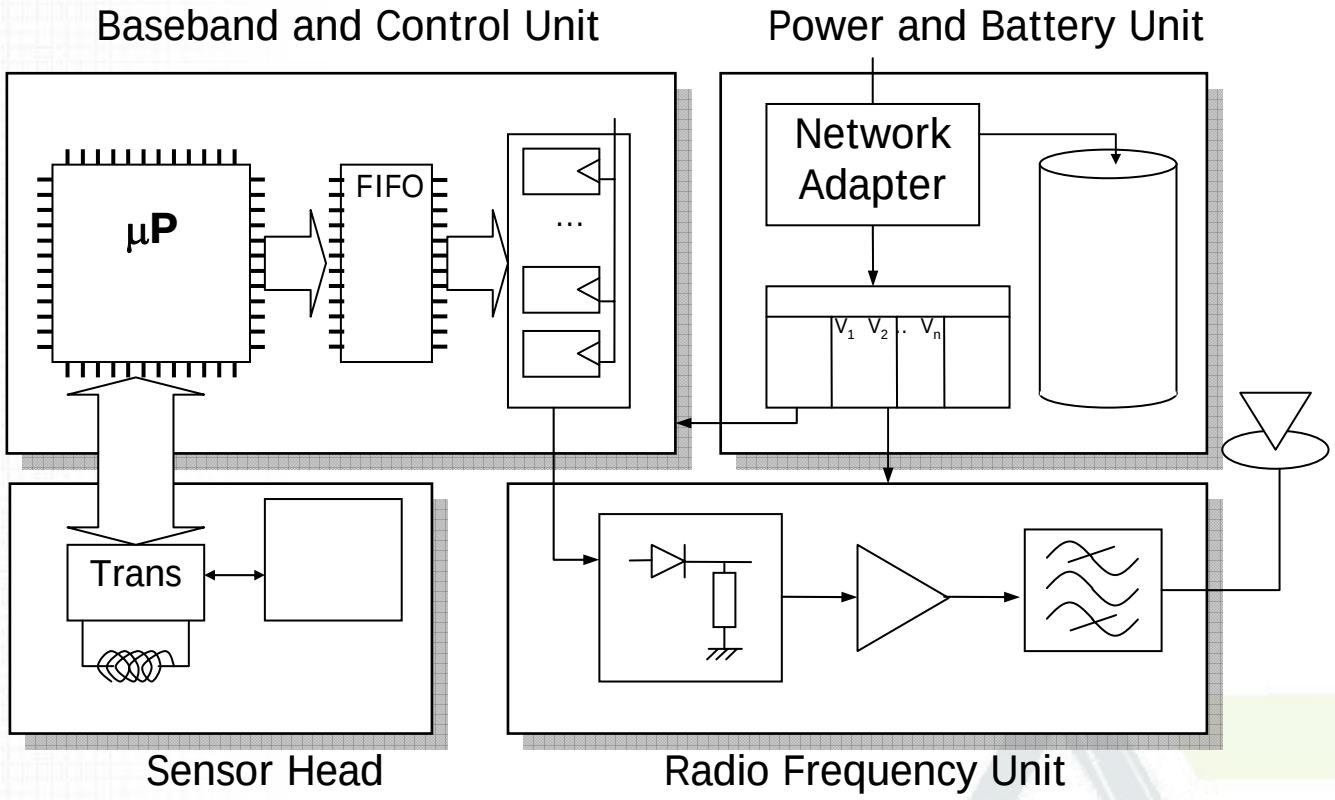


Sensor Heads

- Research hot topic nowadays
  - Passive sensors
  - MEMS based (fuel & vapour sensors)
  - Biological and chemical
    - Bacteria based:
      - Contaminant detection (ligth emitting bacteria)
      - Explosives detection (protein production with TNT)

Transmitter Architecture

- Transmitter schematic

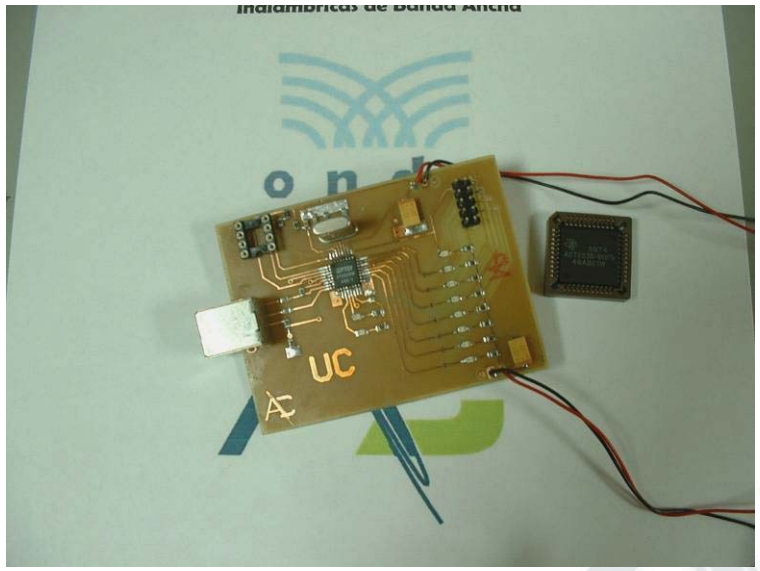


Transmitter Architecture Key Elements

- Digital processor:
  - Power consumption < 20mA @ 3.3V
- GALI Pulse amplifier
  - Wide bandwidth
  - Good matching
  - High gain

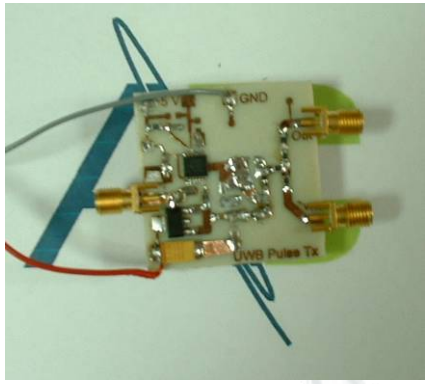
Transmitter design

- Control PC Tx/Rx interface→ USB
  - Packet based transmission (LDR)
  - 1 Kb Packet transmission
    - Header: Synchronización, MAC, Networking…
    - Data



Transmitter Design

- Asynchronous PC Interface; PC ↔ UWB Tx
  - 8 bitWords serie USB → Paralell
  - FIFO + Shift Register
  - 1024 bits Word → Serie
    - PRF : 13 MHz
- Pulse generator:
  - 1) Step Recovery Diode based.



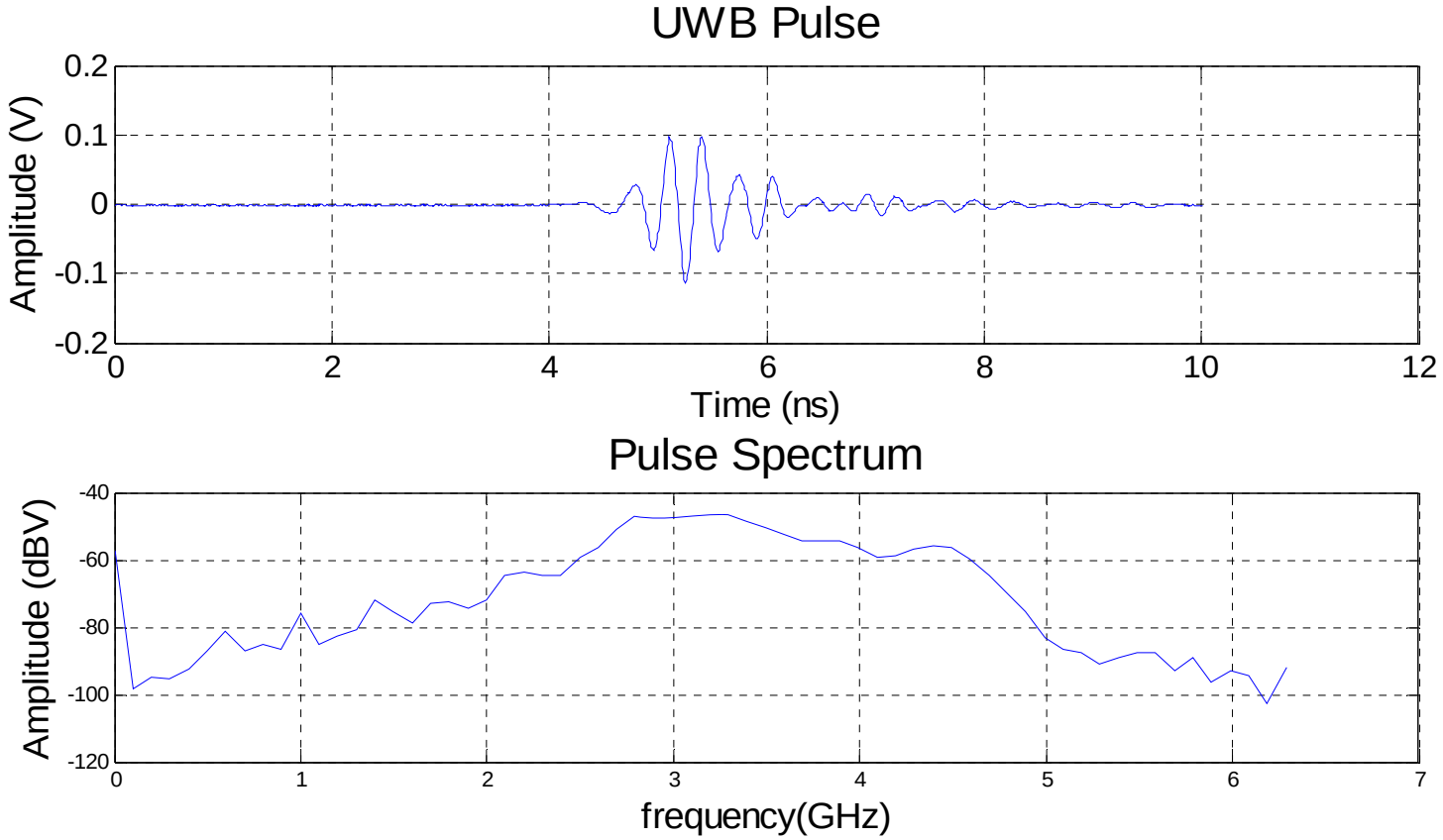
  - 2) High Speed Logic Device (under development)

TX Signal Characteristics

- Parameters
  - Bandwidth (@10 dB) ~ 1.5 - 2 GHz
  - Center Frequency ~ 4 GHz
  - Power Spectral Density ~ -41 dBm/MHz
  - Tx power: 0.16 W → 22 dBm
  - Pulse Width ~ 300 ps
- Alternatives:
  - Generated pulse filtering
  - Frequency conversion

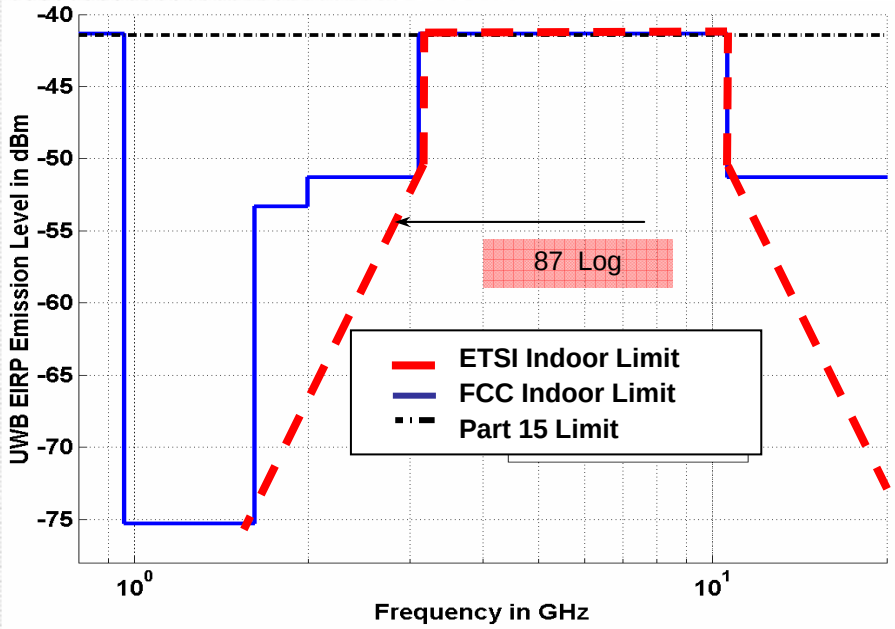
UWB Signal Filtering

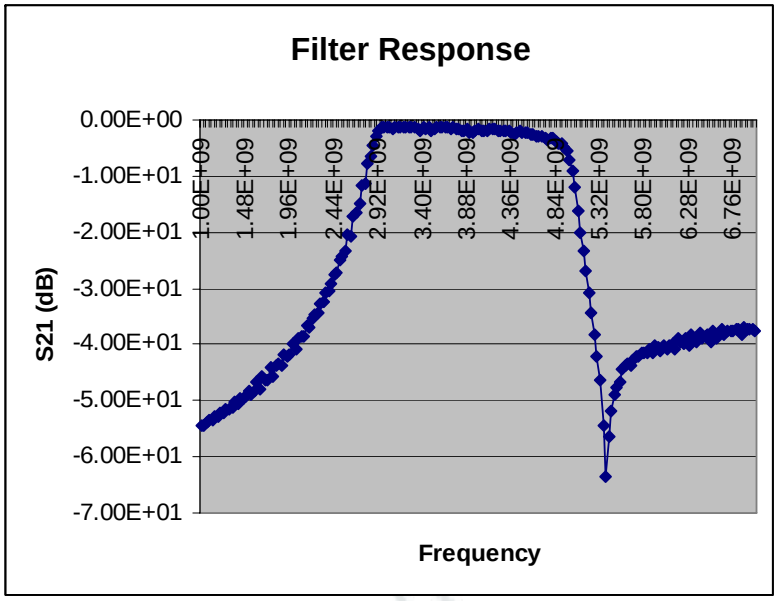
- UWB Generated Signal → Filter components out of channel



Filtering

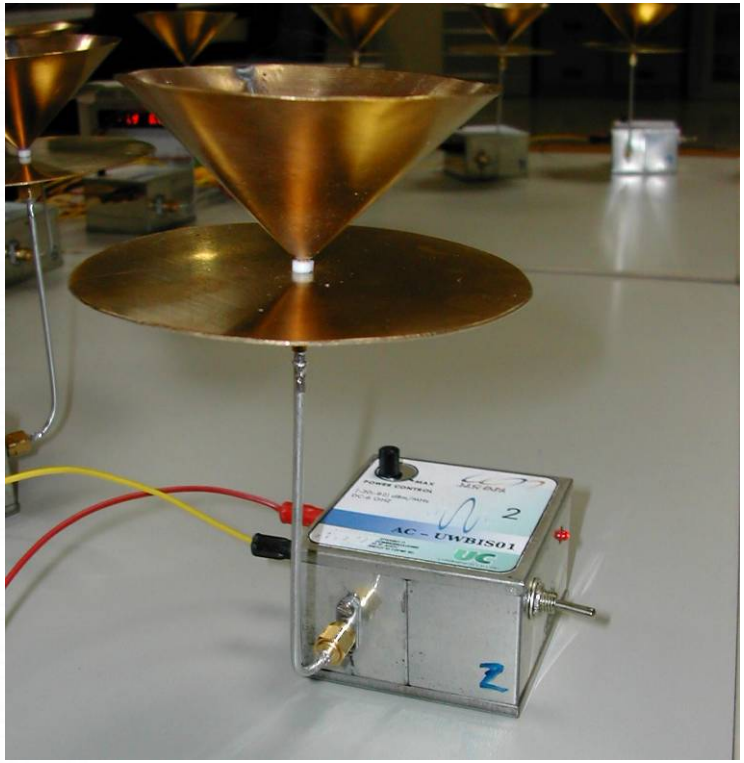
- Microstrip Filter 3 to 5 GHz





TX Design

- Amplifier and RF filter
- Antenna

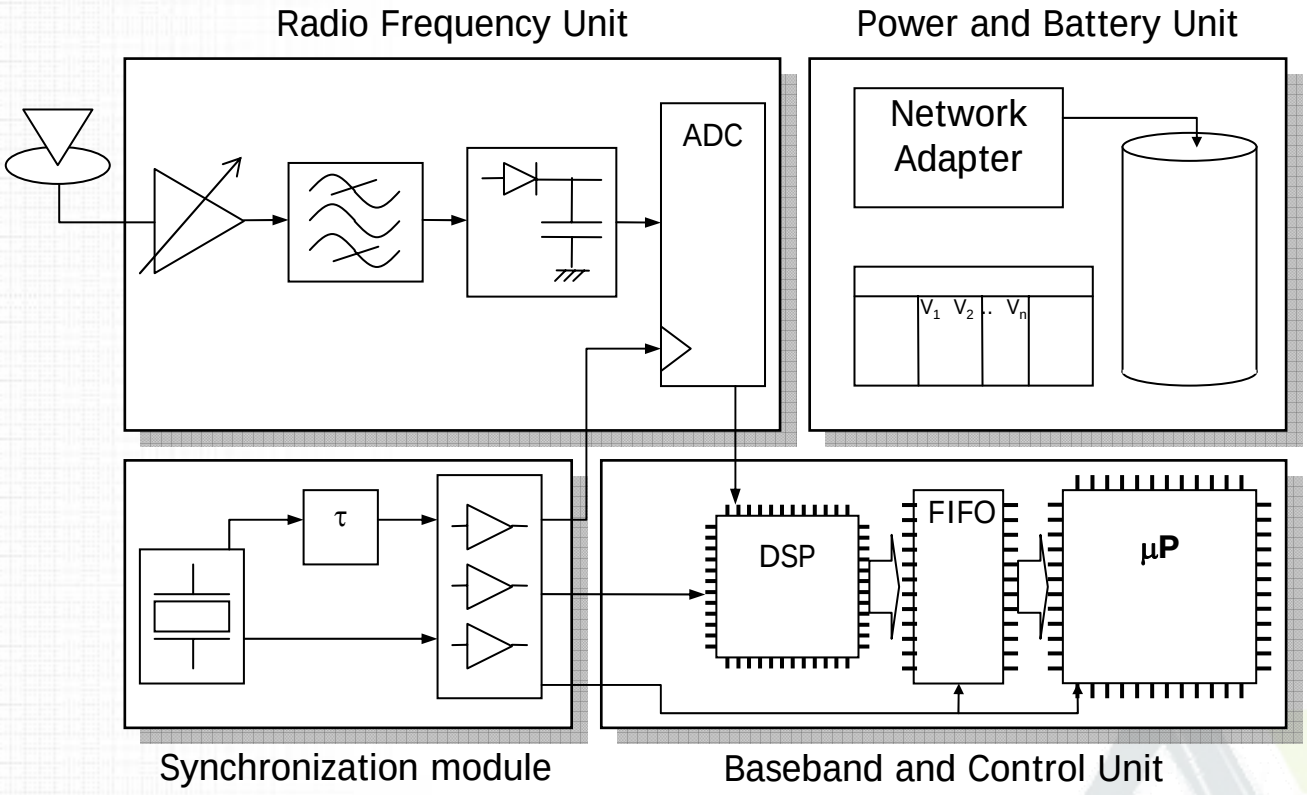


Receiver Architecture Architectre

- Receiver based on:
  - Low Noise Amplifier
  - Filter
  - Pulse Energy Detection
  - Low Power ADC
  - Synchronization module
  - Micro-processor for demodulation

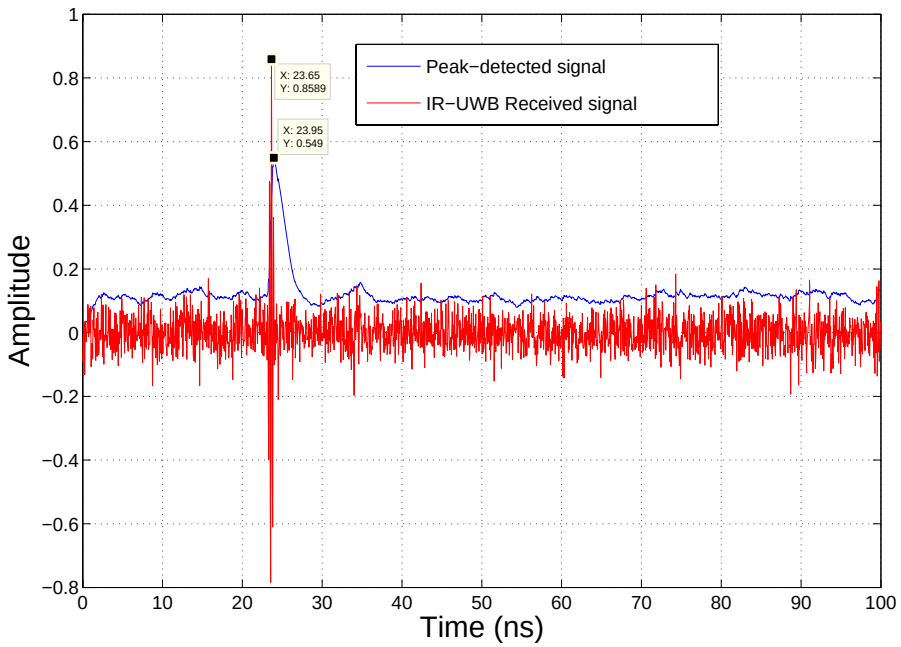
Receiver Architecture Architectre

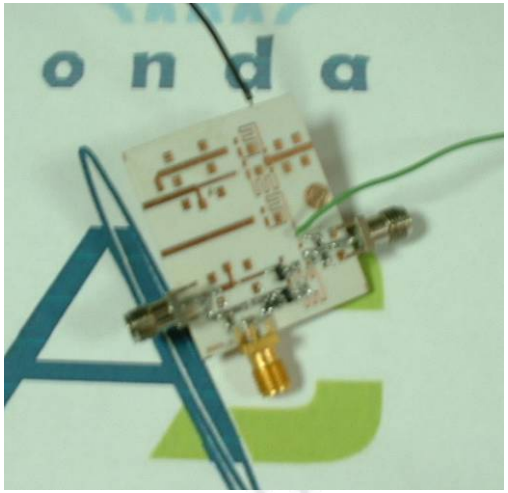
- Receiver Schematic



RF Receiver

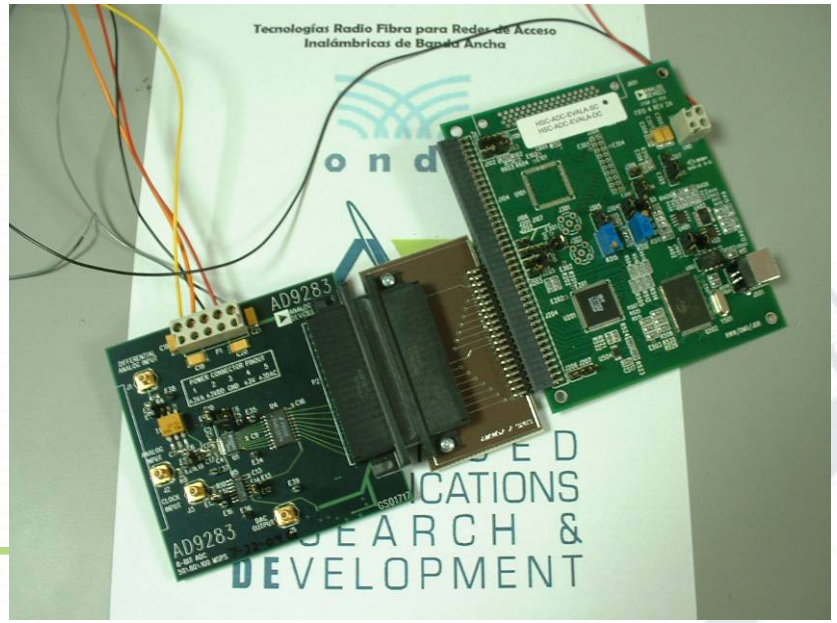
- Pulse Detection
  - Peak Detector (Schottky diode)





RF – BB Interface

- ADC: AD92XX series (8 bits)
  - BW: 475 MHz
  - Sample Frequency < 100 MHz
  - 8 nsec pulse --> Not enough!!
    - Solution: Delay line + DSP



Synchonism

– DSP connected to ADC output

Receiver – PC Interface

- Same structure as in transmission
  - DSP controls FIFO writes (once synchonised)
  - FIFO ↔ USB
  - USB ↔ PC

Positioning & Localisation

- Reference points
- Range based algorithms
  - RSSI → Signal strength
  - TOA → Time differences
- Combination!